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February 6, 2006

From: Curtis A. Vock

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To:	Company:	Fax Number:	Phone Number:
Mail Stop: Appeal Brief -- Patents	U.S. Patent Office	(571) 273-8300	

Number of Pages Transmitted (including this cover sheet): 16

Message:

Applicant(s)	S. Brandon Keller, et al.	Examiner	Naum B. Levin
Serial No.	10/647,594	Group Art No.	2825
Filed	August 25, 2003	Confirmation No.	2408
For	Systems and Methods for Determining Activity Factors of a Circuit Design		

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IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): S. Brandon Keller, et al.

Application No.: 10/647,594

Filing Date: Aug. 25, 2003

Title: Systems And Methods For Determining Activity Factors Of A Circuit Design

Confirmation No.: 2408

Examiner: Naum B. Levin

Group Art Unit: 2825

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Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on __Dec. 6, 2005__.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $500.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

( ) one month	$120.00	
( ) two months	$450.00	
( ) three months	$1020.00	
( ) four months	$1590.00	

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of __$500.00__. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

( ) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Alexandria, VA 22313-1450. Date of Deposit:_____
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Number of pages: 16

Typed Name: Janet Ridpath

Signature: _____

Respectfully submitted,

S. Brandon Keller, et al.

By _____

William A. Rudy
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IN THE UNITED STATES PATENT OFFICE

Applicant(s)	S. Brandon Keller, et al.		Examiner	Naum B. Levin
Serial No.	10/647,594		Group Art No.	2825
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For	Systems and Methods for Determining Activity Factors of a Circuit Design			

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

In accord with 37 CRF § 41.37, and fully responsive to the Office Action of September 6, 2005, Appellants hereby file this appeal brief in support of their Appeal in the above-identified U.S. Application No. 10/647,594 (hereinafter the '594 Application). A notice of appeal, with appropriate fee of $500 as required by §§41.31, 41.20(b)(1), was filed on December 6, 2005. The $500 fee for this appeal brief, as required by 37 CRF §41.20(b)(2), is also filed herewith. This appeal brief is timely filed within two months of the mailing of the notice of appeal.

(1)   Real party in interest.

The real party in interest for this appeal is Hewlett-Packard Development Company, L.P. (HPDC), a limited partnership established under the laws of the State of Texas and having a principal place of business at 20555 S.H. 249, Houston, TX 77070, U.S.A. HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware Corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, L.L.C. Evidence of this

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assignment, which was recorded on October 7, 2003, may be found at reel/frame 014029/0997.

(2)   **Related appeals and interferences.**

No other appeals or interferences are currently known to Appellants that will directly affect, be directly affected by, or have a bearing on the decision to be rendered by the Board of Patent Appeals and Interferences in the present appeal.

(3)   **Status of claims.**

Claims 1-20 are pending in the '594 Application. Claims 1-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,668,732 ("Khouja"). Applicants appeal all claims 1-20.

(4)   **Status of amendments.**

The '594 Application was filed on August 25, 2003. A first office action was mailed on April 28, 2005, to which a response was filed and entered on June 20, 2005. On September 6, 2005, a final rejection was mailed, prompting the notice of appeal filed on December 6, 2005. Claims 1-20 are currently pending, all of which are original (without claim amendment during prosecution).

(5)   **Summary of claimed subject matter.**

The '594 Application discloses, for example, a method for determining activity factors for signal nets of a circuit design. An activity factor is assigned to one or more node types. Signal nets of the circuit design are matched to the one or more node types to determine an activity factor. See paragraphs [0019], [0020] and table 1 of the '594 Application. Specifically, the node type of the signal net determines the activity factor to be applied to the signal net. Using the example of FIG. 2, circuit recognition tool 122 determines a node type for each net (NET A-F) within netlist 118' by matching each net to one or more node types. Analysis tool 120 determines an activity factor for each net by looking up the determined node type for the net in activity factor lookup table 124.

Analysis tool 120 then utilizes this activity factor when analyzing the net. See paragraphs [0021]-[0022].

With this background, claims 1-5 in particular relate to a method for determining activity factors of a circuit design. See, e.g., FIG. 4 and FIG. 5 and corresponding text in paragraphs 26-29 in the specification. Claims 6-10 and claims 11-14 relate to systems for determining activity factors of a circuit design. See, e.g., FIG. 1 and corresponding text in paragraphs 14-20 of the specification. Claims 15-20 relate to a software product that performs steps for determining activity factors of a circuit design. See, e.g., paragraph 8 and FIG. 4 and FIG. 5.

Claims 2, 10, 12 and 16 recite node types of static, dynamic, clock and non-toggling, and taught for example by paragraphs [0019] and [0020], table 1 and FIG. 2 of the '594 Application.

Claims 3, 8 and 18 recite the use of a lookup table for storing activity factors associated with node types, such as taught for example by paragraphs [0020-23] and activity factor lookup table 124 in FIGs. 1 and 2.

Claims 4, 5 and 19 recite that switching power is determined based upon activity factors, determined from node types of the signal nets, such as taught for example by at least paragraphs [0019], [0021-22] and [0029].

Claim 7 requires that the analysis tool be responsive to the E-CAD tool to analyze the circuit design, such as taught by paragraphs [0016] and [0017].

Claims 9, 13, 14 and 17 recite that an activity factor is assigned to each of the node types, such as for example taught by paragraphs [0005] and [0020].

(6)   **Grounds for rejection to be reviewed on appeal.**

Whether claims 1-20 are anticipated by Khouja in accordance 35 U.S.C. §102(b).

(7)   **Arguments.**

Claim 1 of the '594 Application recites a method for determining activity factors of a circuit design, including steps of:

a) assigning an activity factor to one or more node types;

b) reading one or more signal nets from a netlist of the circuit design;

c) processing the signal nets to associate one of the node types with each of the signal nets; and

d) determining an activity factor for each of the signal nets based upon node type.

Step a) of claim 1 requires that an activity factor be assigned to one or more node types. For example, paragraph [0019] of the '594 Application recites "a node type may be static, dynamic, clock or non-toggling." Paragraph [0020] and table 1 of the '594 Application illustrate that an activity factor is assigned to one or more node types. For example, table 1 shows that an activity factor of 0.2 is assigned to node type dynamic.

On the other hand, Khouja discloses that its process "must also determine the mode of every endpoint net for each level," wherein "these endpoint nets represent inputs of sequential cells or primary output ports." Khouja col. 36, lines 4-7. Khouja continues: "the mode of each such output net defaults to 'sp-only' ... if the net is used to drive any asynchronous logic... the net's mode is set to 'sp-and-tr'." Khouja col. 36, lines 7-11. The *modes* of Khouja are thus entirely different from *node* types of the immediate application.

Steps b) and c) of claim 1 of the '594 Application require that the signal nets are read from a netlist of the circuit design and processed to associate a node type with each signal net. For example, paragraph [0019] of the '594 Application teaches "circuit recognition tool 120 processes the signal nets to determine a node type that most closely resembles the signal net," such that each signal net is processed and categorized as one of the node types.

On the other hand, Khouja does not disclose processing the signal nets to associate one of the node types with each of the signal nets as required by step c), for example. Instead, the modes of Khouja are determined only for endpoint nets of each level. Khouja thus has no disclosure as to matching signal nets to one or more node types.

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Teaching away from claim 1 of the '594 Application, Khouja instead discloses "computing toggle rates for a combinational logic circuit ... toggle rates are first annotated on the primary inputs ... logic function is computed at each net in the circuit ... for each function, Boolean difference functions and their probabilities are computed with respect to each input." See Khouja col. 25 lines 41-64. Clearly, Khouja computes activity factors for signal nets in the circuit based upon toggle rates of the primary inputs and probabilities. Khouja does not assign an activity factor to signal nets based upon an associated node type as required by step d).

In col. 7, lines 35-45, Khouja discloses that a state element graph is constructed for the circuit, cycles are broken in the graph, toggle rates are computed using levels in the state element graph and toggle rates and probabilities are transferred across sequential elements. This is not at all the same as claim 1 of the '594 Application.

At least for these reasons, Khouja cannot anticipate claim 1 under 35 U.S.C. §102(b).

Claim 6 of the '594 Application recites a system for determining activity factors of a circuit design, including elements:

    a) a circuit recognition tool responsive to control by an E-CAD tool to determine node types of one or more signal nets of the circuit design;

    b) memory for storing activity factors associated with the node types, the activity factor being determined by node type; and

    c) an analysis tool being operable to access the memory to determine an activity factor for each of the signal nets based upon node type.

Khouja does not disclose use of a circuit recognition tool for determining node types of one or more signal nets as required by element a) of claim 6. Further, Khouja does not store activity factors associated with node types in memory, as required by element b). Paragraph [0021] and table 1 of the '594 Application describe an exemplary lookup table and FIG. 1 shows one exemplary activity factor lookup table 124. The relationship between node types and activity factors are clearly taught in the '594

Application. Khouja's endpoint nets are not the same as node types associated with activity factors stored within a memory, as in claim 6.

At least for these reasons, Khouja cannot anticipate claim 6 under 35 U.S.C. §102(b).

Claim 11 of the '594 Application recites a system for determining activity factors of a circuit design, including elements of:

    a) means for reading one or more signal nets from a netlist of the circuit design;

    b) means for processing the signal nets to determine a node type for each of the signal nets; and

    c) means for determining an activity factor for each of the signal nets based upon node type.

As argued above, Khouja does not process signal nets to determine a node type for each of the signal nets as required by step b). Further, Khouja does not disclose or suggest determining activity factors for signal nets based upon node type as required by element c). Therefore, Khouja also cannot anticipate claim 11.

Claim 15 of the '594 Application recites a software product with instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining activity factors of a circuit design, including:

    a) reading one or more signal nets from a netlist of the circuit design;

    b) processing the signal nets to associate a node type with each of the signal nets; and

    c) determining an activity factor for each of the signal nets based upon the node type.

Again, as argued above, Khouja does not process signal nets to associate a node type with each of the signal nets as required by step b) of claim 15. Khouja further does not determine and activity factor for each of the signal nets based upon node type.

At least for these reasons, Khouja cannot anticipate claim 15 under 35 U.S.C. §102(b).

Reconsideration of independent claims 1, 6, 11 and 15 is respectfully requested.

Each claim of claims 2-5, 7-10, 12-14 and 16-20 depends from one of these independent claims and benefits from like argument. But these claims also have features that patentably distinguish over Khouja. For example, claim 2 recites determining a node type selected from the group of static, dynamic, clock and non-toggling. Khouja does not disclose determining all of these node types.

Claim 3 recites storing the activity factor within a lookup table. Khouja does not – anywhere – disclose or suggest storing activity factors within a lookup table.   Claim 4 recites determining switching power requirements based upon the activity factor for each of the signal nets; and claim 5 recites using the activity factor assigned to the node type of each of the signal nets. Khouja does not associate activity factors with node types of each signal net.

Claim 7 recites that the analysis tool is responsive to control by the E-CAD tool to analyze the circuit design using the activity factors. Claim 8 recites memory storing an activity factor lookup table and the analysis tool accessing the activity factor lookup table to determine the activity factor for each of the signal nets based upon node type. Khouja again does not disclose or suggest use of a memory for storing an activity factor lookup table, nor an analysis tool that accesses the activity factor lookup table to determine the activity factor for each of the signal nets based upon node type.

Claim 9 recites means for accepting user inputs to specify the activity factors stored in the memory. Claim 10 recites node types that are of static, dynamic, clock and non-toggling. Claim 12 recites means for determining a node type selected from the group of static, dynamic, clock and non-toggling. Claim 13 recites means for assigning an activity factor to each of the node types. Claim 14 recites means for assigning being responsive to user inputs to store activity factors associated with the node types. Claim 16 recites determining a node type selected from the group of static, dynamic, clock and non-toggling. Claim 17 recites assigning an activity factor to each of the node types. Claim 18 recites storing the activity factor within a lookup table. Claim 19 recites determining switching power requirements based upon the activity factors for the signal

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nets. Claim 20 recites reading the activity factor for each of the signal nets. Khouja does not disclose the features of these claims.

Claims 1-20 cannot therefore be anticipated by Khouja; reconsideration is requested.

(8)   Claims Appendix.

Appellants enclose a copy of the claims involved in this appeal as an appendix hereto.

(9)   Evidence Appendix.

No evidence is entered or relied upon in this appeal.

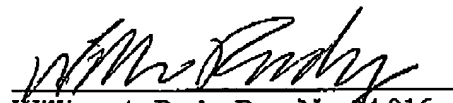**(10)   Related Proceedings Appendix.**

To Appellants' knowledge, there are no decisions rendered by a court or the Board for submission with this appeal.

Conclusions

Appellants respectfully submit that the claims 1-20 patentably distinguish over the art of record. Other than the costs for the appeal brief, we believe no additional fees are due in connection with this matter. However, if any additional fee is deemed necessary, the Commissioner is hereby authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By: _____

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CLAIM APPENDIX TO APPEAL BRIEF

1.   (Original)   A method for determining activity factors of a circuit design, comprising:

     assigning an activity factor to one or more node types;

     reading one or more signal nets from a netlist of the circuit design;

     processing the signal nets to associate one of the node types with each of the signal nets; and

     determining an activity factor for each of the signal nets based upon node type.

2.   (Original)   The method of claim 1, the step of processing comprising determining a node type selected from the group of static, dynamic, clock and non-toggling.

3.   (Original)   The method of claim 1, the step of assigning comprising storing the activity factor within a lookup table.

4.   (Original)   The method of claim 1, further comprising determining switching power requirements based upon the activity factor for each of the signal nets.

5.   (Original)   The method of claim 4, the step of determining switching power requirements comprising using the activity factor assigned to the node type of each of the signal nets.

6.   (Original)   A system for determining activity factors of a circuit design, comprising:

     a circuit recognition tool responsive to control by an E-CAD tool to determine node types of one or more signal nets of the circuit design;

     memory for storing activity factors associated with the node types, the activity factor being determined by node type; and

     an analysis tool being operable to access the memory to determine an activity factor for each of the signal nets based upon node type.

7.   (Original)   The system of claim 6, the analysis tool being responsive to control by the E-CAD tool to analyze the circuit design using the activity factors.

8.   (Original)   The system of claim 6, the memory storing an activity factor lookup table, the analysis tool accessing the activity factor lookup table to determine the activity factor for each of the signal nets based upon node type.

9.   (Original)   The system of claim 6, further comprising means for accepting user inputs to specify the activity factors stored in the memory.

10.   (Original)   The system of claim 6, the node types comprising one of static, dynamic, clock and non-toggling.

11.   (Original)   A system for determining activity factors of a circuit design, comprising:

    means for reading one or more signal nets from a netlist of the circuit design;

    means for processing the signal nets to determine a node type for each of the signal nets; and

    means for determining an activity factor for each of the signal nets based upon node type.

12.   (Original)   The system of claim 11, further comprising means for determining a node type selected from the group of static, dynamic, clock and non-toggling.

13.   (Original)   The system of claim 11, further comprising means for assigning an activity factor to each of the node types.

14.   (Original)   The system of claim 13, the means for assigning being responsive to user inputs to store activity factors associated with the node types.

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15. (Original) A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for determining activity factors of a circuit design, comprising:

reading one or more signal nets from a netlist of the circuit design;

processing the signal nets to associate a node type with each of the signal nets; and

determining an activity factor for each of the signal nets based upon the node type.

16. (Original) The software product of claim 15, further comprising determining a node type selected from the group of static, dynamic, clock and non-toggling.

17. (Original) The software product of claim 15, further comprising assigning an activity factor to each of the node types.

18. (Original) The software product of claim 17, further comprising storing the activity factor within a lookup table.

19. (Original) The software product of claim 15, further comprising determining switching power requirements based upon the activity factors for the signal nets.

20. The software product of claim 19, further comprising reading the activity factor for each of the signal nets.

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Evidence Appendix

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Appeal Brief for U.S. Patent Application Serial No.: 10/205,332

Related Proceedings Appendix

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PAGE 16/16 * RCVD AT 2/6/2006 4:04:52 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/36 * DNIS:2738300 * CSID: * DURATION (mm-ss):07-18